Qualitative Abstraction based Verification for Analog Circuits

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Abstract. The verification of analog designs is a challenging and exhaustive task that requires deep understanding of the physical behaviors. In this paper, we propose a qualitative based predicate abstraction method for the verification of a class of non-linear analog circuits. The method is based on combining techniques from constraint solving and computer algebra along with symbolic model checking. We have implemented the proposed verification algorithms using the computer algebra system Mathematica and the SMV model checker.

1 Introduction

A cornerstone in embedded systems are analog designs, which are integrated circuits, required at the interfaces with the real world environment. Computer aided design (CAD) has been under intense research during the past decades to overcome challenges in the design process of analog designs. For verification purposes, simulation approaches are usually applied to check that a design is robust with respect to different types of inaccuracies. However, with designs growing in complexity, introducing more rigorous verification techniques, complementing simulation is becoming of great importance.

Formal methods like model checking have been advocated for the verification of digital designs where their correctness is proved mathematically against some formal properties. Motivated by the success of the application of formal methods in the verification of digital designs, researchers started investigating the formal verification of analog designs. In analog designs, one is interested in global properties connected to the dynamic behavior of the design. Unlike its digital counterpart, analog designs verification is a challenging and exhaustive task that requires deep understanding of their behavior. Challenging problems like non- linear effects make a direct application of formal methods very difficult and abstraction techniques are required in order to achieve this task. *Predicate abstraction* is one of the most successful abstraction approaches developed in (8), for the verification of systems with infinite state space. In this approach, the state space is divided into a finite set of regions and a set of rules is used to build the transition between these regions in a way that the generated state transition system can be verified using model checking. Among the proposed enhancements of predicate